Bachelor-/Masterarbeit am Fachgebiet Leistungselektronik:

Bearbeitungszeit: 20 Wochen (Bachelorarbeit)/ 26 Wochen (Masterarbeit)
Sprache: Deutsch/Englisch
Start: ab sofort
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Arbeitstitel:
„Layout-Optimierung zur Anwendung mit hohen Frequenzen von GaN-Transistoren mithilfe EM-Simulation“ /
“Layout optimization for high-frequency application of GaN-transistors using EM-simulation”

Motivation:

With the growing requirements for volume, integration and efficiency, GaN devices are increasingly used to design high-efficiency and high-frequency power converters due to their higher switching speed and lower on-resistance. However, with the high \( \frac{dv}{dt} \) and \( \frac{di}{dt} \), small parasitic components can result in severe oscillations, which cause electromagnetic interface issues and even breakdown of devices. The coupling between power-loop and gate-loop result in the ringing of gate-source voltage and may induce false turn-on. Moreover, the parasitic components decrease the switching speed and in turn lead to an increase of loss. In order to utilize the benefits of GaN devices, it is necessary to redesign and optimize the layout to minimize the parasitic components.

The aims of this thesis including:

- Investigation of parasitic components extraction methods
- Redesign and optimize layout in terms of power-loop and gate loop using EM-simulation
- Compare different layout and study their impact on switching transitions
- Implement the new design and verify its benefits by measurements